**What is Claimed is:**

1. An integrated circuit First-In-First-Out (FIFO) memory device comprising:

a FIFO memory that is divisible into up to a predetermined number of independent FIFO queues;

a register file including the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues;

an indexer that is configured to index into the register file to access a respective word that corresponds to a respective FIFO queue that is accessed; and

a controller that is responsive to the respective word that is accessed and that is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

2. An integrated circuit FIFO memory device according to Claim 1 wherein the one or more parameters comprise count parameters and/or flag parameters.

3. An integrated circuit FIFO memory device according to Claim 1 wherein the one or more parameters comprise a number of words read, a number of words written, a number of packets read, a number of packets written, a location of a next word to be read, a location of a next word to be written, a start address and/or an end address for the respective queue.

4. An integrated circuit FIFO memory device according to Claim 1 wherein the one or more parameters comprise mask values that are used to generate a full, almost full and/or almost empty flag for the respective queue.

5. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a plurality of register subfiles, each of which includes the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues; and

wherein the controller comprises a plurality of controller subblocks, a respective one of which is responsive to the respective word that is accessed in at least one of the register subfiles and that is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

6. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a read word counter register subfile including the predetermined number of words, a respective word of which is configured to store a number of words read for a respective one of the FIFO queues; and

wherein the controller comprises a read word counter controller subblock that is responsive to the respective word that is accessed in the read word counter register subfile and that is configured to control reading from the respective FIFO queue based upon the number of words read that is stored in the respective word.

7. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a write word counter register subfile including the predetermined number of words, a respective word of which is configured to store a number of words written into a respective one of the FIFO queues; and

wherein the controller comprises a write word counter controller subblock that is responsive to the respective word that is accessed in the write word counter register subfile and that is configured to control writing into the respective FIFO queue based upon the number of words written that is stored in the respective word.

8. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a read packet counter register subfile including the predetermined number of words, a respective word of which is configured to store a number of packets read for a respective one of the FIFO queues; and

wherein the controller comprises a read packet counter controller subblock that is responsive to the respective word that is accessed in the read packet counter

register subfile and that is configured to control reading from the respective FIFO queue based upon the number of packets read that is stored in the respective word.

9. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a write packet counter register subfile including the predetermined number of words, a respective word of which is configured to store a number of packets written into a respective one of the FIFO queues; and

wherein the controller comprises a write packet counter controller subblock that is responsive to the respective word that is accessed in the write packet counter register subfile and that is configured to control writing into the respective FIFO queue based upon the number of packets written that is stored in the respective word.

10. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a full flag constant latch register subfile including the predetermined number of words, a respective word of which is configured to store at least one mask value that is used to generate a full flag for a respective one of the FIFO queues; and

wherein the controller comprises a full flag constant latch controller subblock that is responsive to the respective word that is accessed in the read word counter register subfile and that is configured to control generating a full flag for the respective FIFO queue based upon the at least one mask value that is stored in the respective word.

11. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a programmable almost full flag constant latch register subfile including the predetermined number of words, a respective word of which is configured to store at least one mask value that is used to generate a programmable almost full flag for a respective one of the FIFO queues; and

wherein the controller comprises a programmable almost full flag constant latch controller subblock that is responsive to the respective word that is accessed in the read word counter register subfile and that is configured to control generating a programmable almost full flag for the respective FIFO queue based upon the at least one mask value that is stored in the respective word.

12. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a programmable almost empty flag constant latch register subfile including the predetermined number of words, a respective word of which is configured to store at least one mask value that is used to generate a programmable almost empty flag for a respective one of the FIFO queues; and

wherein the controller comprises a programmable almost empty flag constant latch controller subblock that is responsive to the respective word that is accessed in the read word counter register subfile and that is configured to control generating a programmable almost empty flag for the respective FIFO queue based upon the at least one mask value that is stored in the respective word.

13. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a read data path counter register subfile including the predetermined number of words, a respective word of which is configured to store a physical memory location of a next word to be read for a respective one of the FIFO queues; and

wherein the controller comprises a read data path counter controller subblock that is responsive to the respective word that is accessed in the read data path counter register subfile and that is configured to control reading from the respective FIFO queue based upon the physical memory location of a next word to be read that is stored in the respective word.

14. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a write data path counter register subfile including the predetermined number of words, a respective word of which is configured to store a physical memory location of a next word to be written for a respective one of the FIFO queues; and

wherein the controller comprises a write data path counter controller subblock that is responsive to the respective word that is accessed in the write data path counter register subfile and that is configured to control writing into the respective FIFO queue based upon the physical memory location of a next word to be written that is stored in the respective word.

15. An integrated circuit FIFO memory device according to Claim 1:

wherein the register file comprises a start/end register subfile including the predetermined number of words, a respective word of which is configured to store physical memory locations of a start and an end of a respective one of the FIFO queues; and

wherein the controller comprises a start/end controller subblock that is responsive to the respective word that is accessed in the start/end register subfile and that is configured to control reading from and writing to the respective FIFO queue based upon the physical memory locations of a start and an end that is stored in the respective word.

16. An integrated circuit FIFO memory device according to Claim 1 wherein the indexer comprises a word address decoder.

17. An integrated circuit FIFO memory device according to Claim 1 wherein the controller comprises an incrementer that is configured to selectively increment the one or more parameters.

18. An integrated circuit FIFO memory device according to Claim 1 wherein the controller comprises a comparator that is configured to compare a current address to an end address and an incrementer that is configured to selectively increment the one or more parameters based on comparison results from the comparator.

19. An integrated circuit FIFO memory device according to Claim 1 wherein the controller comprises at least one latch that is configured to latch at least one of the one or more parameters for the respective FIFO queue.

20. An integrated circuit FIFO memory device according to Claim 1 wherein the controller comprises at least one decoder that is responsive to the respective word that is accessed.

21. An integrated circuit First-In-First-Out (FIFO) memory device comprising:

a FIFO memory;

a data input port;

a data output port;

a FIFO controller that is configured to operate the FIFO memory as from one up to a predetermined number greater than one of independent FIFO queues;

a data input system that is configured to write input data from the input port into a first selected one of the independent FIFO queues; and

a data output system that is configured to read data from a second selected one of the independent FIFO queues.

22. An integrated circuit FIFO memory device according to Claim 21 wherein the FIFO controller stores therein one or more parameters for each of the up to a predetermined number of independent FIFO queues and is configured to control writing of the input data into the first selected one of the independent FIFO queues based upon at least one of the one or more parameters that is stored for the first selected one of the independent FIFO queues and to control reading of data from the second selected one of the independent FIFO queues based upon at least one of the one or more parameters that is stored for the second selected one of the independent FIFO queues.

23. An integrated circuit FIFO memory device according to Claim 21 wherein the one or more parameters comprise a number of words read, a number of words written, a number of packets read, a number of packets written, a location of a next word to be read, a location of a next word to be written, a start address and/or an end address for the respective FIFO queue.

24. An integrated circuit FIFO memory device according to Claim 21 wherein the one or more parameters comprise mask values that are used to generate a full, almost full and/or almost empty flag for the respective FIFO queue.

25. An integrated circuit FIFO memory device according to Claim 21 wherein the first and second selected ones of the independent FIFO queues are different ones of the independent FIFO queues.

26. An integrated circuit FIFO memory device according to Claim 21 wherein the FIFO controller comprises:

a register file including the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues;

an indexer that is configured to index into the register file to access a respective word that corresponds to a respective FIFO queue that is accessed; and

wherein the controller is responsive to the respective word that is accessed and is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

27. An integrated circuit FIFO memory device according to Claim 21 wherein the FIFO memory comprises an embedded memory device and a multi-port cache memory device.

28. An integrated circuit First-In-First-Out (FIFO) memory device comprising:

a FIFO memory including a predetermined number, greater than one of FIFO queues;

a register file including the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues;

an indexer that is configured to index into the register file to access a respective word that corresponds to a respective FIFO queue that is accessed; and

a controller that is responsive to the respective word that is accessed and that is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

29. An integrated circuit FIFO memory device according to Claim 28 wherein the one or more parameters comprise count parameters and/or flag parameters.

30. An integrated circuit FIFO memory device according to Claim 28 wherein the one or more parameters comprise a number of words read, a number of words written, a number of packets read, a number of packets written, a location of a next word to be read, a location of a next word to be written, a start address and/or an end address for the respective queue.

31. An integrated circuit FIFO memory device according to Claim 28 wherein the one or more parameters comprise mask values that are used to generate a full, almost full and/or almost empty flag for the respective queue.

32. An integrated circuit FIFO memory device according to Claim 28:

wherein the register file comprises a plurality of register subfiles, each of which includes the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues; and

wherein the controller comprises a plurality of controller subblocks, a respective one of which is responsive to the respective word that is accessed in at least one of the register subfiles and that is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

33. A method of operating an integrated circuit First-In-First-Out (FIFO) memory device including a FIFO memory containing a predetermined number of independent FIFO queues, the method comprising:

indexing into a register file that includes the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues, to access a respective word that corresponds to a respective FIFO queue that is accessed; and

controlling access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word that is accessed.

34. A method according to Claim 33 wherein the one or more parameters comprise count parameters and/or flag parameters.

35. A method according to Claim 33 wherein the one or more parameters comprise a number of words read, a number of words written, a number of packets read, a number of packets written, a location of a next word to be read, a location of a next word to be written, a start address and/or an end address for the respective queue.

36. A method according to Claim 33 wherein the one or more parameters comprise mask values that are used to generate a full, almost full and/or almost empty flag for the respective queue.

37. A method according to Claim 33:

wherein the indexing comprises indexing into a plurality of register subfiles, each of which includes the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues.

38. A method according to Claim 33 wherein the controlling comprises selectively incrementing the one or more parameters.

39. A method according to Claim 33 wherein the controlling comprises comparing a current address to an end address and selectively incrementing the one or more parameters based on the comparing.

40. A method according to Claim 33 wherein the indexing is preceded by:

dividing the FIFO memory into up to the predetermined number of independent FIFO queues.